FIG. 1

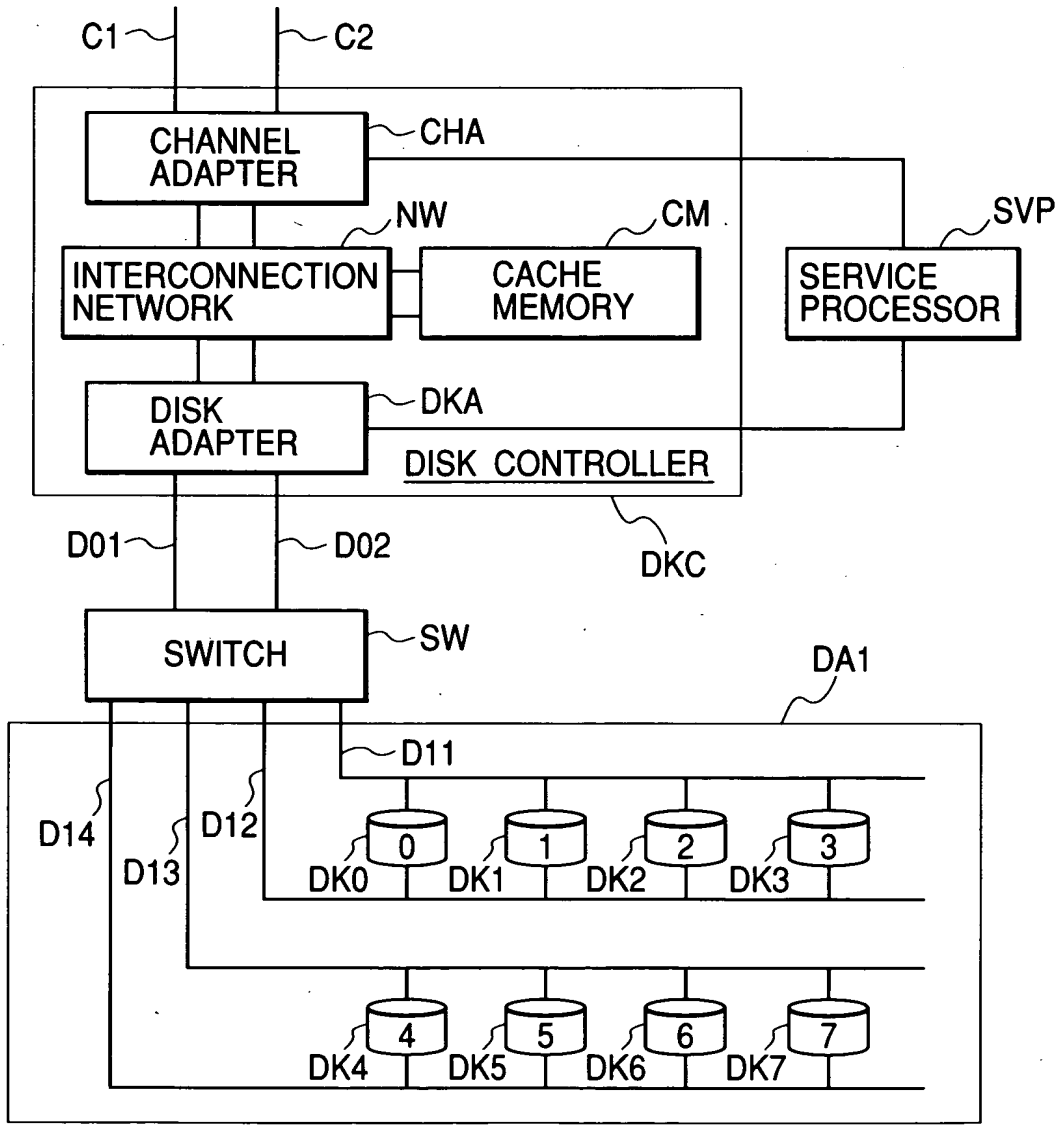
C1
C2
CHANNEL ADAPTER
CHA
NW
CM
SVP
INTERCONNECTION NETWORK
CACHE MEMORY
SERVICE PROCESSOR
DISK ADAPTER
DKA
DISK CONTROLLER
DKC
D01
D02
SWITCH
SW
DA1
D11
D14
D13
D12
0
1
2
3
DK0
DK1
DK2
DK3
4
5
6
7
DK4
DK5
DK6
DK7

FIG. 2

CONFIGURATION OF CHANNEL ADAPTER CHA

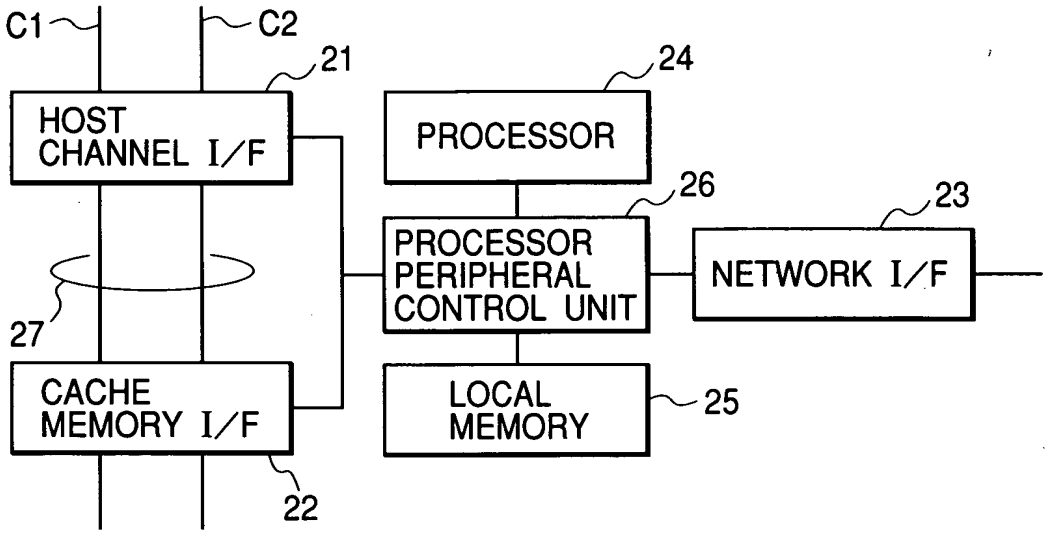

FIG. 3

CONFIGURATION OF DISK ADAPTER DKA

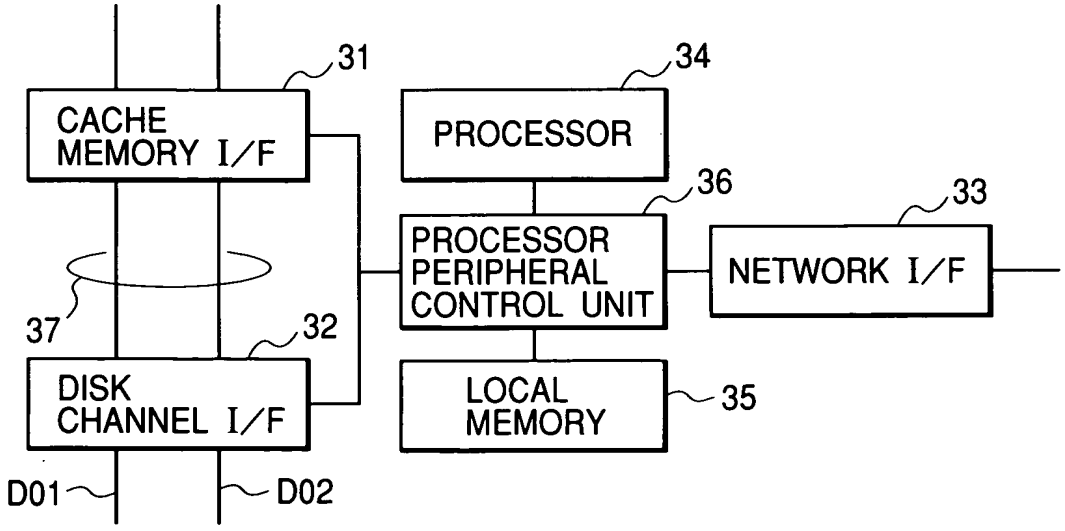

FIG. 4

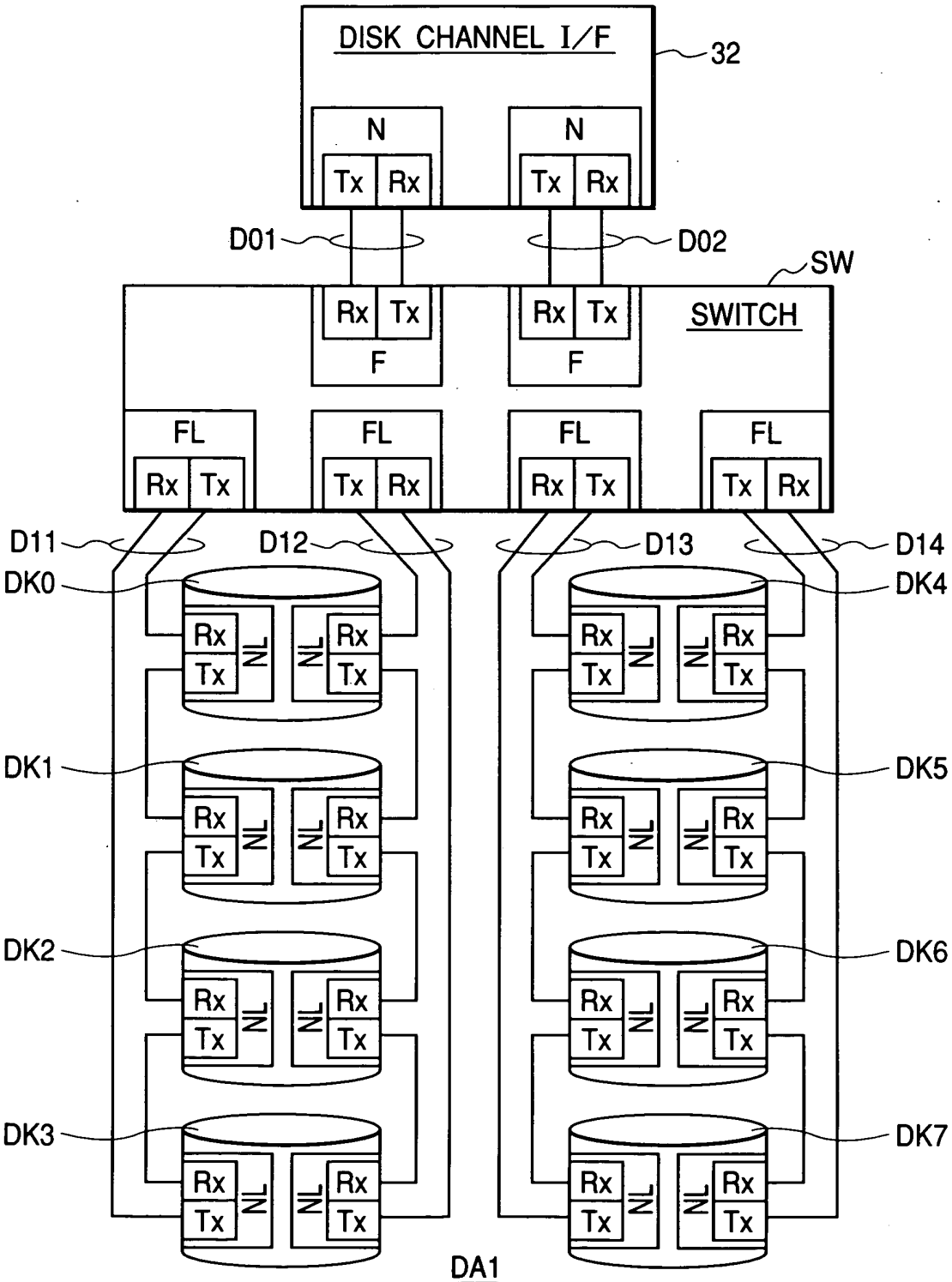
DISK CHANNEL I/F
32
N
Tx
Rx
D01
D02
SW
SWITCH
F
FL
D11
D12
D13
D14
DK0
DK1
DK2
DK3
DK4
DK5
DK6
DK7
NL
DA1

FIG. 5

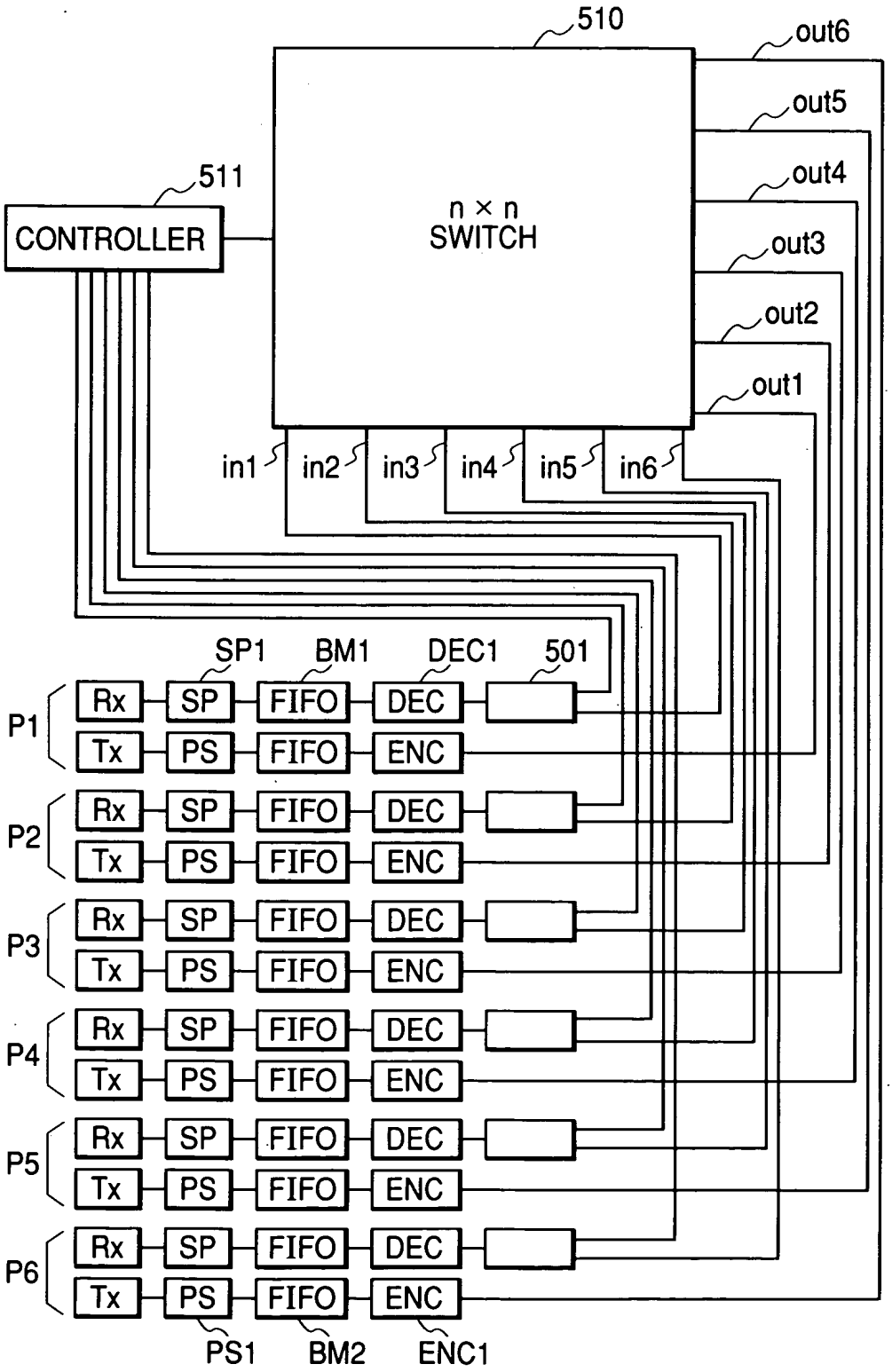
510
out6
out5
out4
out3
out2
out1
511
CONTROLLER
n × n
SWITCH
in1
in2
in3
in4
in5
in6
SP1
BM1
DEC1
501
P1
P2
P3
P4
P5
P6
Rx
Tx
SP
PS
FIFO
DEC
ENC
PS1
BM2
ENC1

FIG. 6

	601		602		603	
	WITHOUT FAILURE		WHEN PORT "a" FAILS		WHEN PORT "b" FAILS	
DRIVE NO.	Read	Write	Read	Write	Read	Write
0	PID_0. a	PID_0. b	PID_0. b		PID_0. a	
1	PID_1. a	PID_1. b	PID_1. b		PID_1. a	
2	PID_2. a	PID_2. b	PID_2. b		PID_2. a	
3	PID_3. a	PID_3. b	PID_3. b		PID_3. a	
4	PID_4. a	PID_4. b	PID_4. b		PID_4. a	
5	PID_5. a	PID_5. b	PID_5. b		PID_5. a	
6	PID_6. a	PID_6. b	PID_6. b		PID_6. a	
7	PID_7. a	PID_7. b	PID_7. b		PID_7. a	

FIG. 7

	701					
	WITHOUT FAILURE		WHEN PORT "a" FAILS		WHEN PORT "b" FAILS	
DRIVE NO.	Read	Write	Read	Write	Read	Write
0	PID_0. a	PID_0. b	PID_0. b		PID_0. a	
1	PID_1. b	PID_1. a	PID_1. b		PID_1. a	
2	PID_2. a	PID_2. b	PID_2. b		PID_2. a	
3	PID_3. b	PID_3. a	PID_3. b		PID_3. a	
4	PID_4. a	PID_4. b	PID_4. b		PID_4. a	
5	PID_5. b	PID_5. a	PID_5. b		PID_5. a	
6	PID_6. a	PID_6. b	PID_6. b		PID_6. a	
7	PID_7. b	PID_7. a	PID_7. b		PID_7. a	

FIG. 8

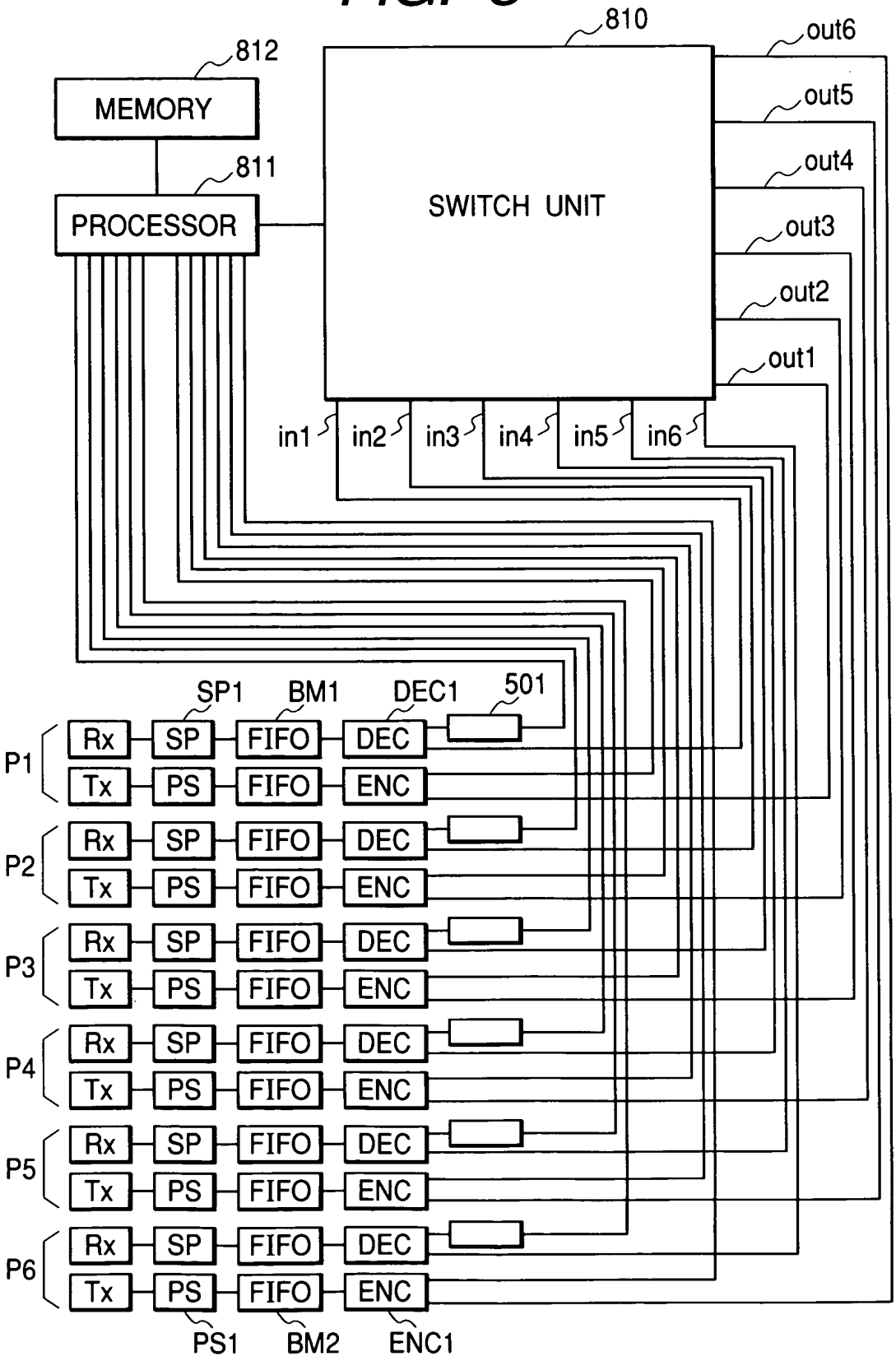
810
812
MEMORY
811
PROCESSOR
SWITCH UNIT
out6
out5
out4
out3
out2
out1
in1
in2
in3
in4
in5
in6
SP1
BM1
DEC1
501
P1
P2
P3
P4
P5
P6
Rx
Tx
SP
PS
FIFO
DEC
ENC
PS1
BM2
ENC1

FIG. 9

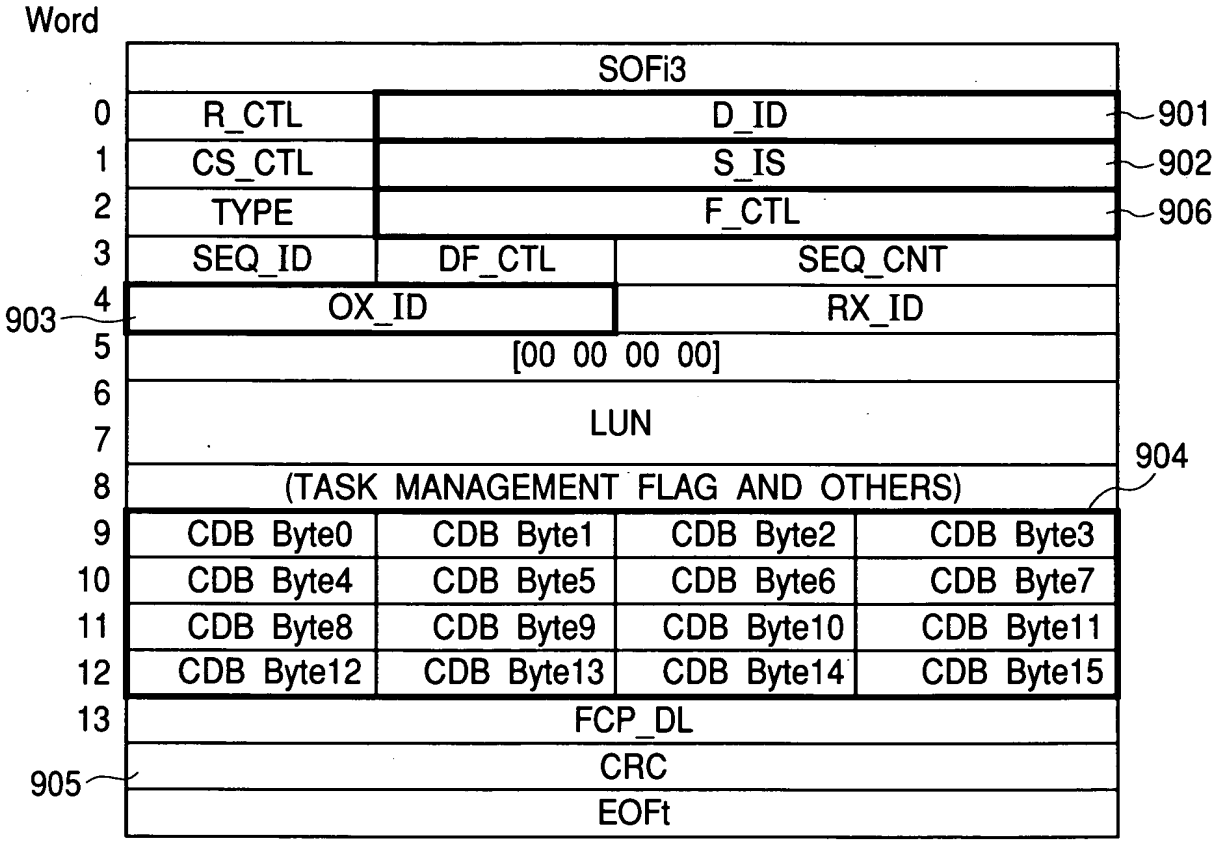
Word
SOFi3
0
R_CTL
D_ID
901
1
CS_CTL
S_IS
902
2
TYPE
F_CTL
906
3
SEQ_ID
DF_CTL
SEQ_CNT
4
903
OX_ID
RX_ID
5
[00 00 00 00]
6
7
LUN
8
(TASK MANAGEMENT FLAG AND OTHERS)
904
9
CDB Byte0
CDB Byte1
CDB Byte2
CDB Byte3
10
CDB Byte4
CDB Byte5
CDB Byte6
CDB Byte7
11
CDB Byte8
CDB Byte9
CDB Byte10
CDB Byte11
12
CDB Byte12
CDB Byte13
CDB Byte14
CDB Byte15
13
FCP_DL
905
CRC
EOFt

FIG. 10

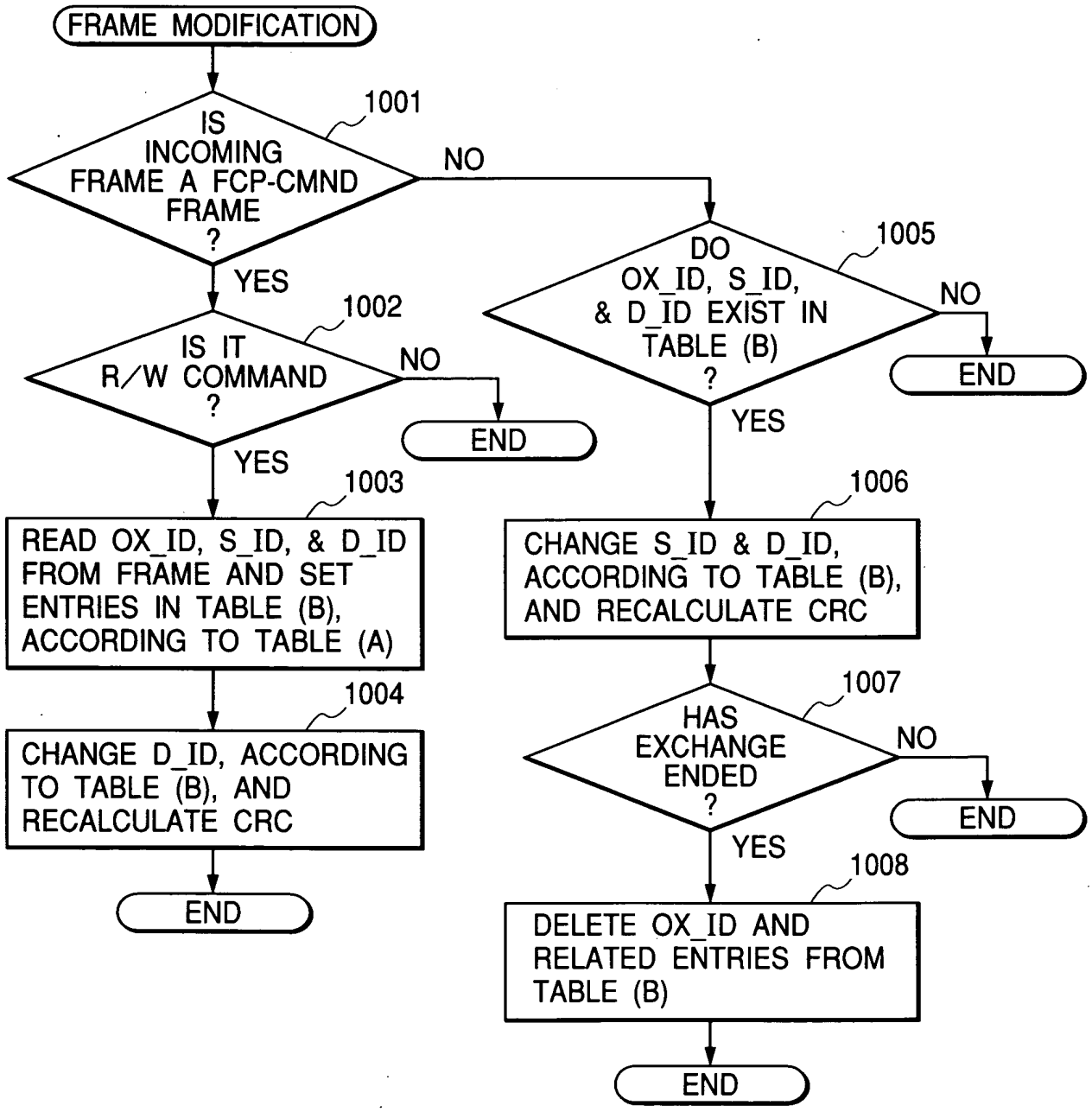
FRAME MODIFICATION
1001
IS INCOMING FRAME A FCP-CMND FRAME ?
NO
YES
1002
IS IT R/W COMMAND ?
NO
END
YES
1003
READ OX_ID, S_ID, & D_ID FROM FRAME AND SET ENTRIES IN TABLE (B), ACCORDING TO TABLE (A)
1004
CHANGE D_ID, ACCORDING TO TABLE (B), AND RECALCULATE CRC
END
1005
DO OX_ID, S_ID, & D_ID EXIST IN TABLE (B) ?
NO
END
YES
1006
CHANGE S_ID & D_ID, ACCORDING TO TABLE (B), AND RECALCULATE CRC
1007
HAS EXCHANGE ENDED ?
NO
END
YES
1008
DELETE OX_ID AND RELATED ENTRIES FROM TABLE (B)
END

FIG. 11A

Drive Port_ID (1101)	Read (1102)	Write (1103)
PID_0.a	PID_0.a	PID_0.b
PID_0.b	PID_0.a	PID_0.b
PID_1.a	PID_1.a	PID_1.b
PID_1.b	PID_1.a	PID_1.b
PID_2.a	PID_2.a	PID_2.b
PID_2.b	PID_2.a	PID_2.b
PID_3.a	PID_3.a	PID_3.b
PID_3.b	PID_3.a	PID_3.b
PID_4.a	PID_4.a	PID_4.b
PID_4.b	PID_4.a	PID_4.b

FIG. 11B

	BEFORE MODIFICATION (1105)		(1106)	AFTER MODIFICATION (1107)		(1108)
	OX_ID (1104)	S_ID	D_ID	S_ID	D_ID	
1109	0x03F2	a	b	WITHOUT CHANGE	c	
1110	0x03F2	c	a	b	WITHOUT CHANGE	
	0x03F3	a	e	WITHOUT CHANGE	f	
	0x03F3	f	a	e	WITHOUT CHANGE	

FIG. 12

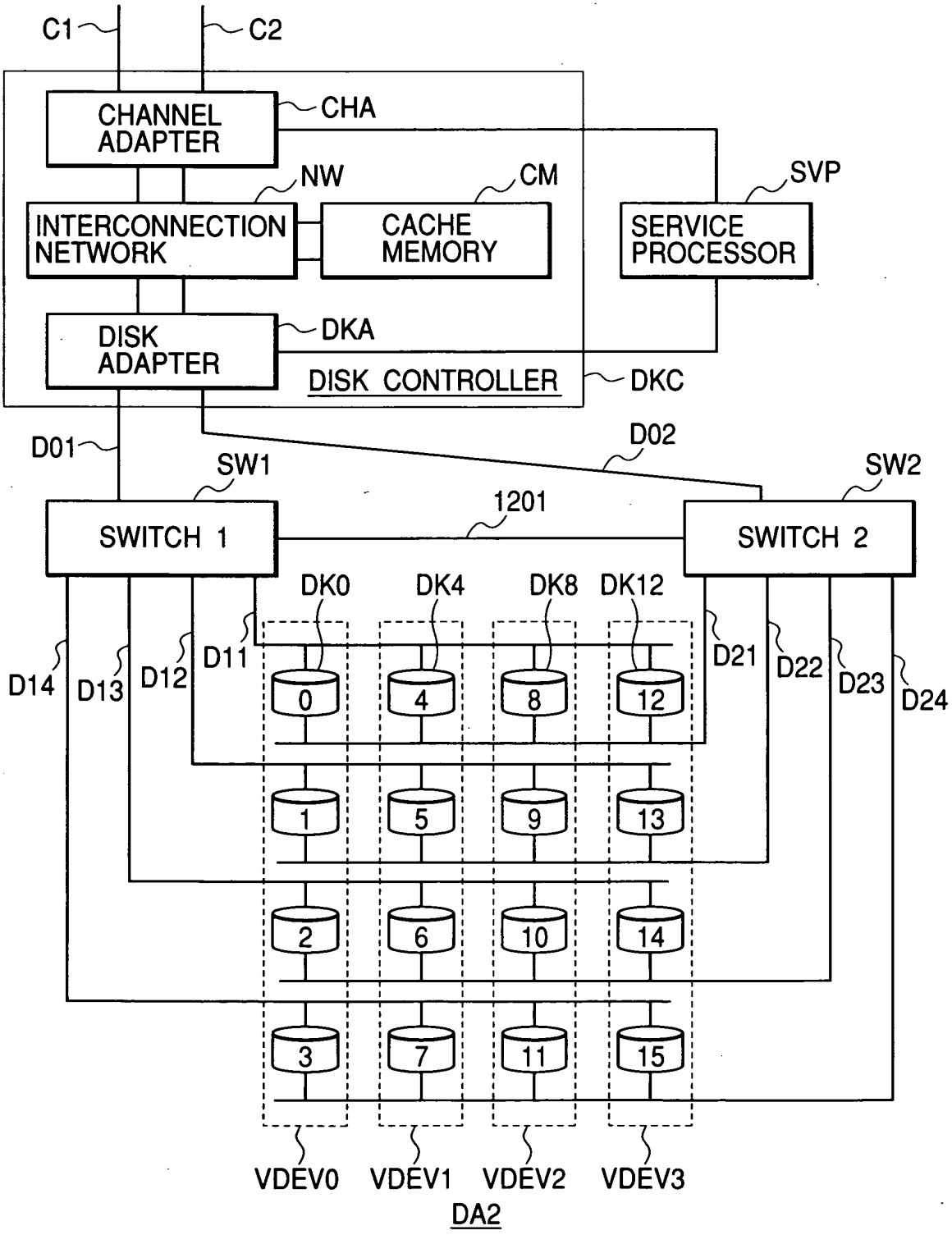
C1
C2
CHANNEL ADAPTER
CHA
NW
CM
SVP
INTERCONNECTION NETWORK
CACHE MEMORY
SERVICE PROCESSOR
DISK ADAPTER
DKA
DISK CONTROLLER
DKC
D01
D02
SW1
SW2
1201
SWITCH 1
SWITCH 2
DK0
DK4
DK8
DK12
D14
D13
D12
D11
D21
D22
D23
D24
0
4
8
12
1
5
9
13
2
6
10
14
3
7
11
15
VDEV0
VDEV1
VDEV2
VDEV3
DA2

FIG. 13

1301		1302			1303		1304	
		WITHOUT FAILURE			WHEN SW1 FAILS		WHEN SW2 FAILS	
DRIVE NO.	VDEV	DKA Port	Read Drive Port	Write Drive Port	DKA Port	R/W Drive Port	DKA Port	R/W Drive Port
0	0	0	PID_0. a	PID_0. b	1	PID_0. b	0	PID_0. a
1			PID_1. a	PID_1. b		PID_1. b		PID_1. a
2			PID_2. a	PID_2. b		PID_2. b		PID_2. a
3			PID_3. a	PID_3. b		PID_3. b		PID_3. a
4	1	0	PID_4. a	PID_4. b	1	PID_4. b	0	PID_4. a
5			PID_5. a	PID_5. b		PID_5. b		PID_5. a
6			PID_6. a	PID_6. b		PID_6. b		PID_6. a
7			PID_7. a	PID_7. b		PID_7. b		PID_7. a
8	2	0	PID_8. a	PID_8. b	1	PID_8. b	0	PID_8. a
9			PID_9. a	PID_9. b		PID_9. b		PID_9. a
10			PID_10. a	PID_10. b		PID_10. b		PID_10. a
11			PID_11. a	PID_11. b		PID_11. b		PID_11. a
12	3	0	PID_12. a	PID_12. b	1	PID_12. b	0	PID_12. a
13			PID_13. a	PID_13. b		PID_13. b		PID_13. a
14			PID_14. a	PID_14. b		PID_14. b		PID_14. a
15			PID_15. a	PID_15. b		PID_15. b		PID_15. a

FIG. 14A

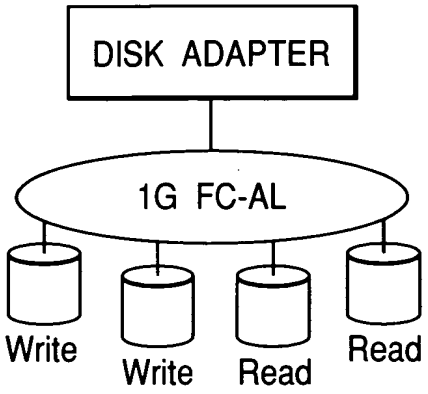

FIG. 14B

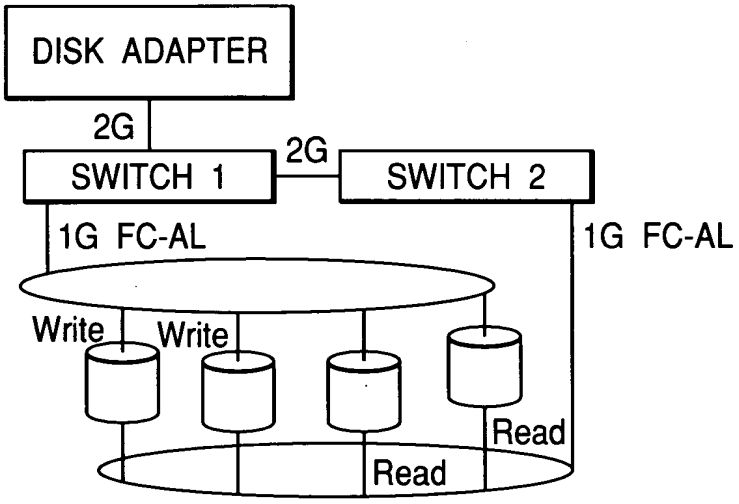

FIG. 14C

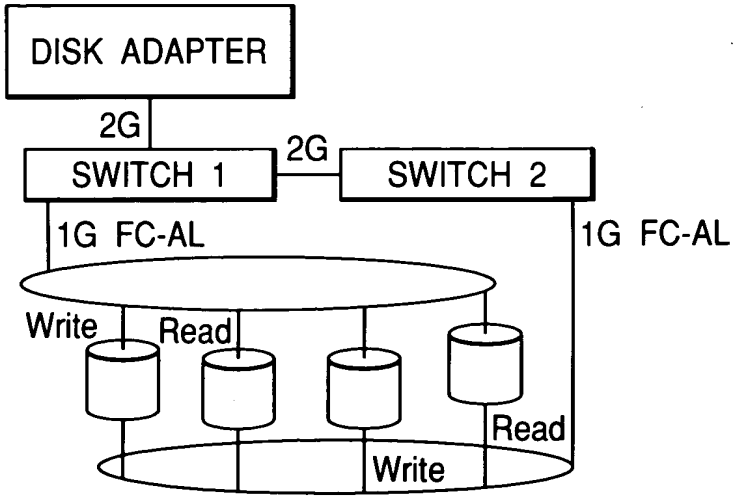

FIG. 15

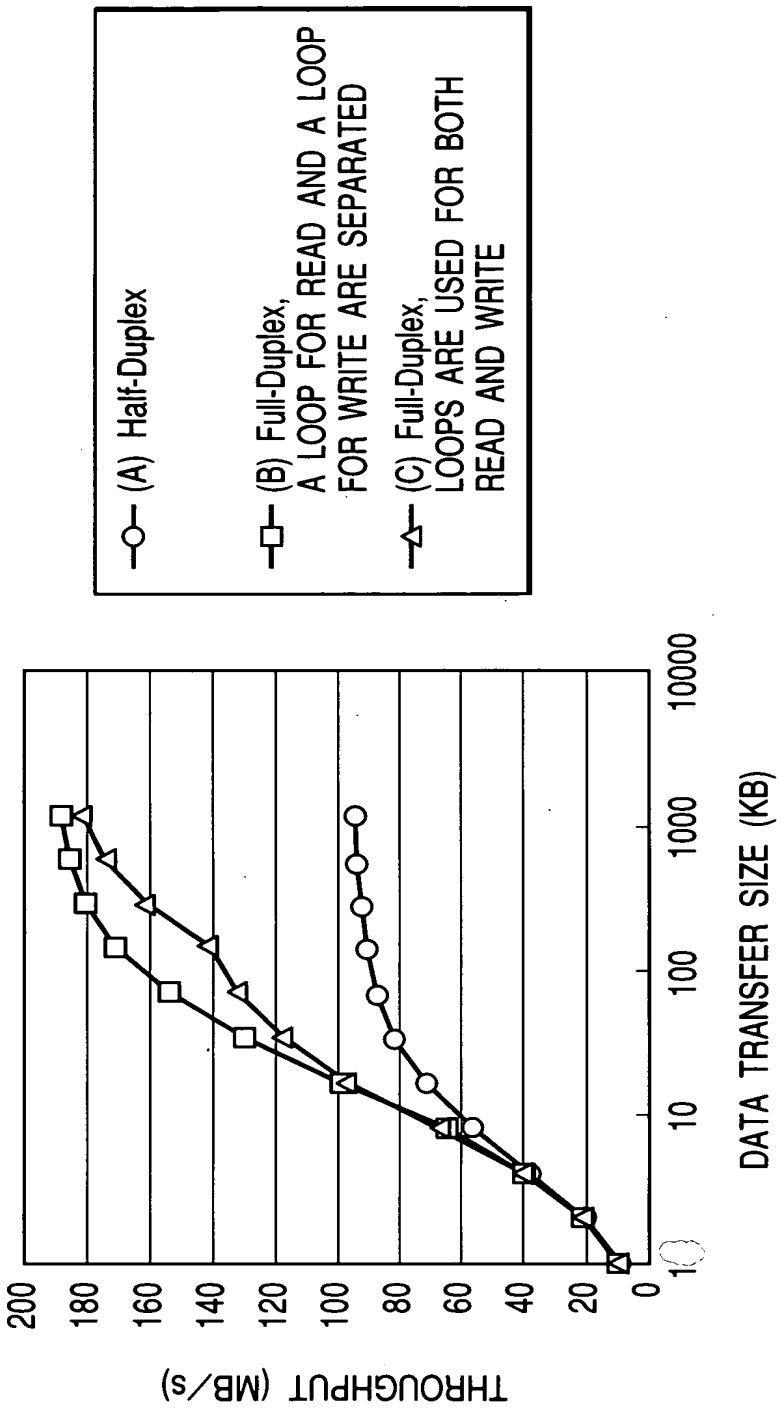
(A) Half-Duplex
(B) Full-Duplex, A LOOP FOR READ AND A LOOP FOR WRITE ARE SEPARATED
(C) Full-Duplex, LOOPS ARE USED FOR BOTH READ AND WRITE
THROUGHPUT (MB/s)
200
180
160
140
120
100
80
60
40
20
0
1
10
100
1000
10000
DATA TRANSFER SIZE (KB)

FIG. 16

1601

		WITHOUT FAILURE			WHEN SW1 FAILS		WHEN SW2 FAILS	
DRIVE NO.	VDEV	DKA Port	Read Drive Port	Write Drive Port	DKA Port	R/W Drive Port	DKA Port	R/W Drive Port
0	0	0	PID_0. a	PID_0. b	1	PID_0. b	0	PID_0. a
1			PID_1. a	PID_1. b		PID_1. b		PID_1. a
2			PID_2. a	PID_2. b		PID_2. b		PID_2. a
3			PID_3. a	PID_3. b		PID_3. b		PID_3. a
4	1	1	PID_4. a	PID_4. b	1	PID_4. b	0	PID_4. a
5			PID_5. a	PID_5. b		PID_5. b		PID_5. a
6			PID_6. a	PID_6. b		PID_6. b		PID_6. a
7			PID_7. a	PID_7. b		PID_7. b		PID_7. a
8	2	0	PID_8. a	PID_8. b	1	PID_8. b	0	PID_8. a
9			PID_9. a	PID_9. b		PID_9. b		PID_9. a
10			PID_10. a	PID_10. b		PID_10. b		PID_10. a
11			PID_11. a	PID_11. b		PID_11. b		PID_11. a
12	3	1	PID_12. a	PID_12. b	1	PID_12. b	0	PID_12. a
13			PID_13. a	PID_13. b		PID_13. b		PID_13. a
14			PID_14. a	PID_14. b		PID_14. b		PID_14. a
15			PID_15. a	PID_15. b		PID_15. b		PID_15. a

FIG. 17

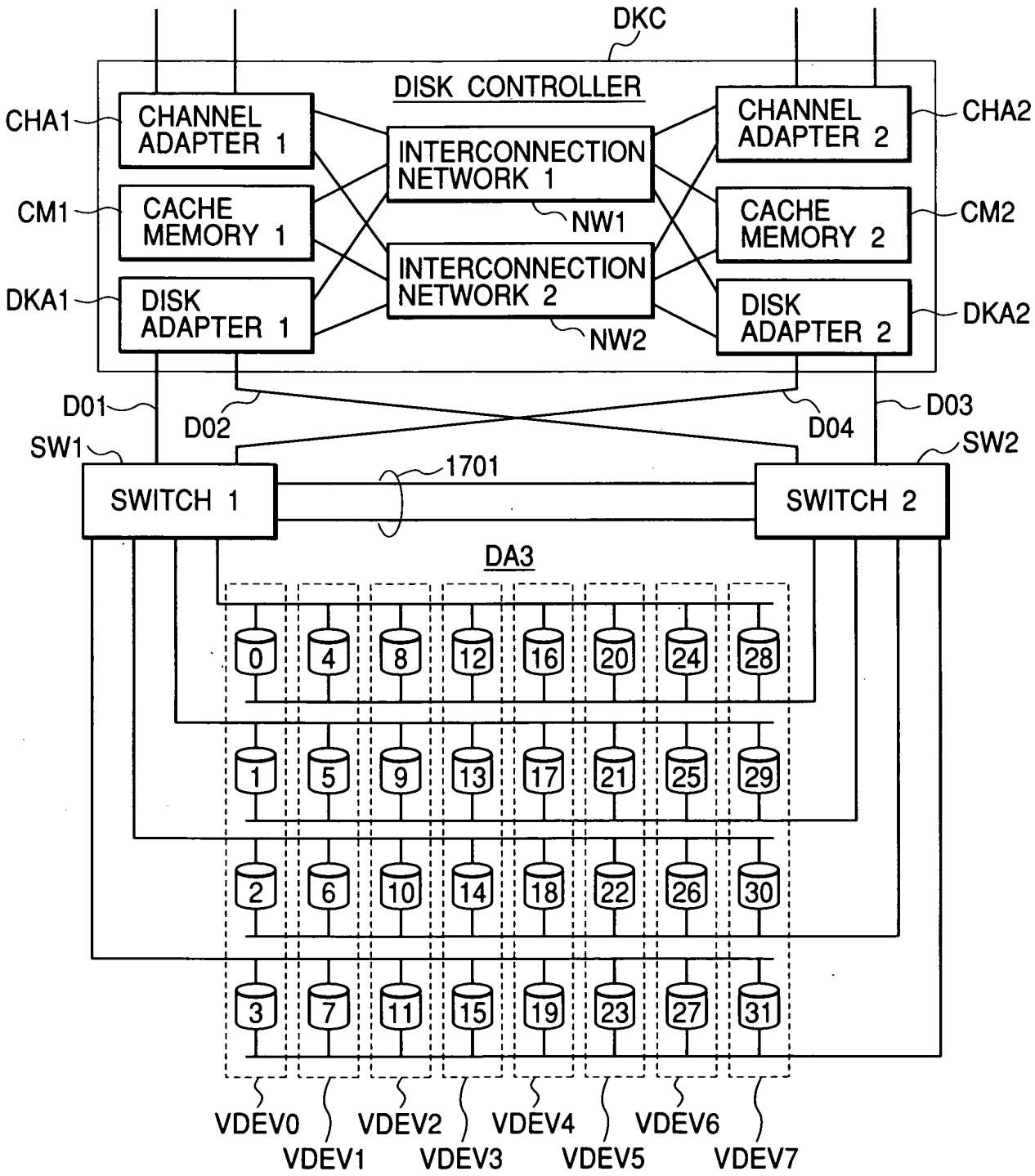
DKC
DISK CONTROLLER
CHA1
CHANNEL ADAPTER 1
CHANNEL ADAPTER 2
CHA2
INTERCONNECTION NETWORK 1
NW1
CM1
CACHE MEMORY 1
CACHE MEMORY 2
CM2
INTERCONNECTION NETWORK 2
NW2
DKA1
DISK ADAPTER 1
DISK ADAPTER 2
DKA2
D01
D02
D04
D03
SW1
SW2
1701
SWITCH 1
SWITCH 2
DA3
0 4 8 12 16 20 24 28
1 5 9 13 17 21 25 29
2 6 10 14 18 22 26 30
3 7 11 15 19 23 27 31
VDEV0
VDEV1
VDEV2
VDEV3
VDEV4
VDEV5
VDEV6
VDEV7

FIG. 18

1801

			WITHOUT FAILURE			WHEN SW1 FAILS		WHEN SW2 FAILS	
DRIVE NO.	VDEV	DKA NO.	DKA Port	Read Drive Port	Write Drive Port	DKA Port	R/W Drive Port	DKA Port	R/W Drive Port
0	0	0	0	PID_0. a	PID_0. b	1	PID_0. b	0	PID_0. a
1				PID_1. a	PID_1. b		PID_1. b		PID_1. a
2				PID_2. a	PID_2. b		PID_2. b		PID_2. a
3				PID_3. a	PID_3. b		PID_3. b		PID_3. a
4	1	1	0	PID_4. a	PID_4. b	0	PID_4. b	1	PID_4. a
5				PID_5. a	PID_5. b		PID_5. b		PID_5. a
6				PID_6. a	PID_6. b		PID_6. b		PID_6. a
7				PID_7. a	PID_7. b		PID_7. b		PID_7. a
8	2	0	1	PID_8. a	PID_8. b	1	PID_8. b	0	PID_8. a
9				PID_9. a	PID_9. b		PID_9. b		PID_9. a
10				PID_10. a	PID_10. b		PID_10. b		PID_10. a
11				PID_11. a	PID_11. b		PID_11. b		PID_11. a
12	3	1	1	PID_12. a	PID_12. b	0	PID_12. b	1	PID_12. a
13				PID_13. a	PID_13. b		PID_13. b		PID_13. a
14				PID_14. a	PID_14. b		PID_14. b		PID_14. a
15				PID_15. a	PID_15. b		PID_15. b		PID_15. a
16	4	0	0	PID_16. a	PID_16. b	1	PID_16. b	0	PID_16. a
17				PID_17. a	PID_17. b		PID_17. b		PID_17. a
18				PID_18. a	PID_18. b		PID_18. b		PID_18. a
19				PID_19. a	PID_19. b		PID_19. b		PID_19. a
20	5	1	0	PID_20. a	PID_20. b	0	PID_20. b	1	PID_20. a
21				PID_21. a	PID_21. b		PID_21. b		PID_21. a
22				PID_22. a	PID_22. b		PID_22. b		PID_22. a
23				PID_23. a	PID_23. b		PID_23. b		PID_23. a
24	6	0	1	PID_24. a	PID_24. b	1	PID_24. b	0	PID_24. a
25				PID_25. a	PID_25. b		PID_25. b		PID_25. a
26				PID_26. a	PID_26. b		PID_26. b		PID_26. a
27				PID_27. a	PID_27. b		PID_27. b		PID_27. a
28	7	1	1	PID_28. a	PID_28. b	0	PID_28. b	1	PID_28. a
29				PID_29. a	PID_29. b		PID_29. b		PID_29. a
30				PID_30. a	PID_30. b		PID_30. b		PID_30. a
31				PID_31. a	PID_31. b		PID_31. b		PID_31. a

FIG. 19

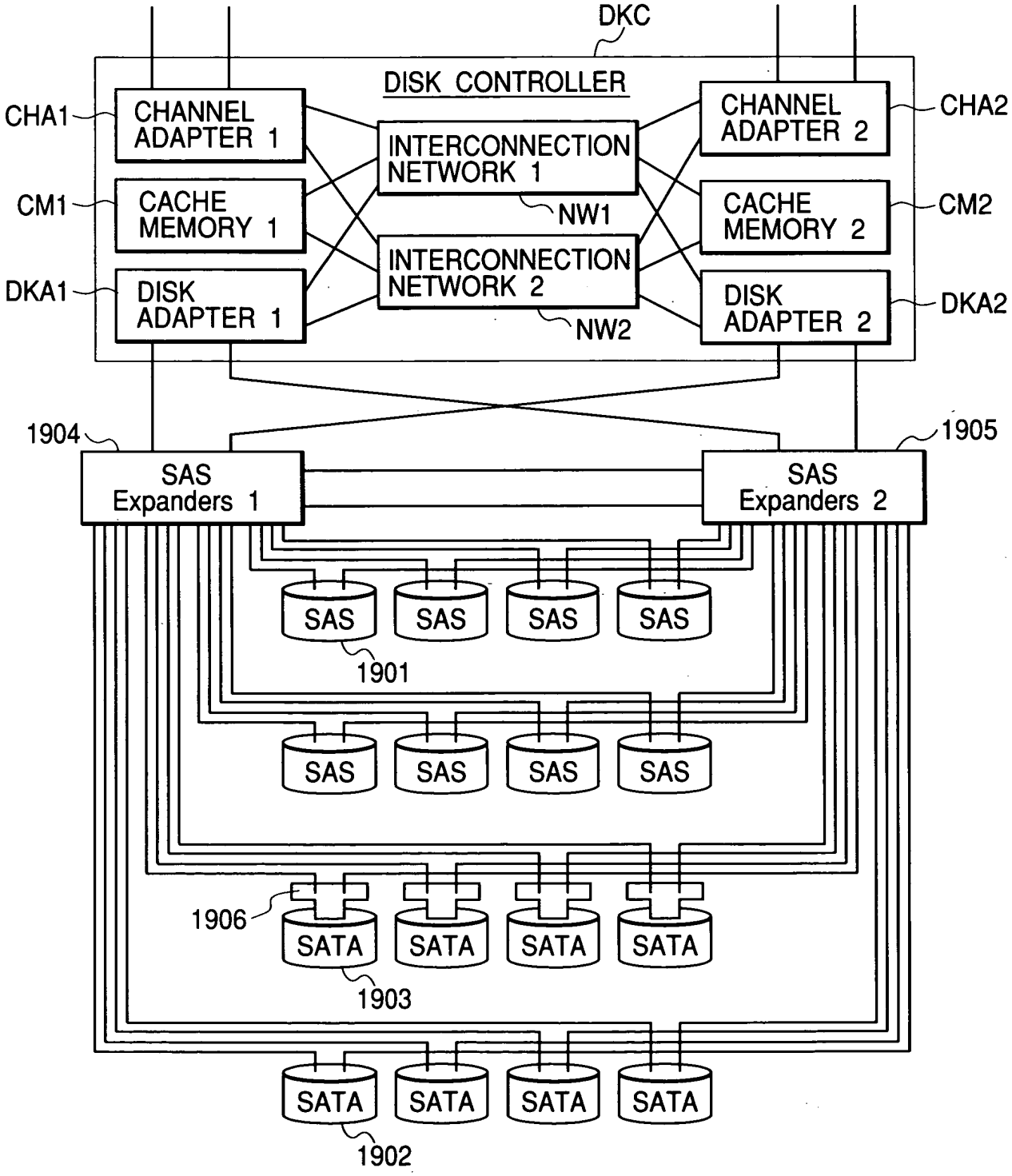
DKC
DISK CONTROLLER
CHA1
CHANNEL ADAPTER 1
CHANNEL ADAPTER 2
CHA2
INTERCONNECTION NETWORK 1
NW1
CM1
CACHE MEMORY 1
CACHE MEMORY 2
CM2
INTERCONNECTION NETWORK 2
NW2
DKA1
DISK ADAPTER 1
DISK ADAPTER 2
DKA2
1904
1905
SAS Expanders 1
SAS Expanders 2
SAS
1901
1906
SATA
1903
1902

FIG. 20

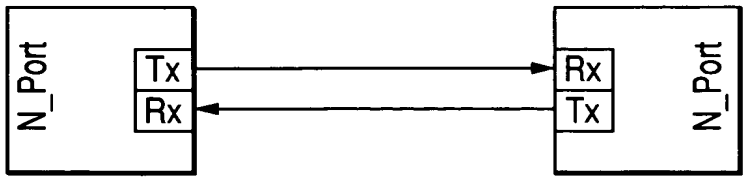

FIG. 21

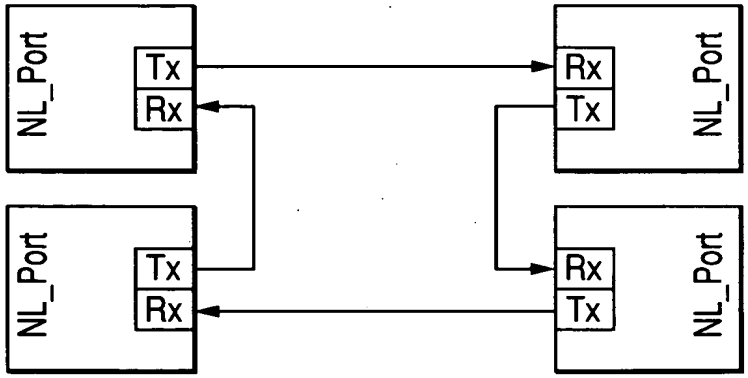

FIG. 22

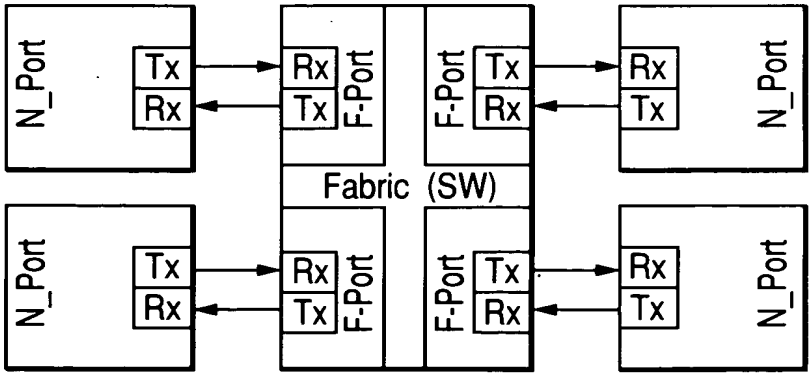

FIG. 23

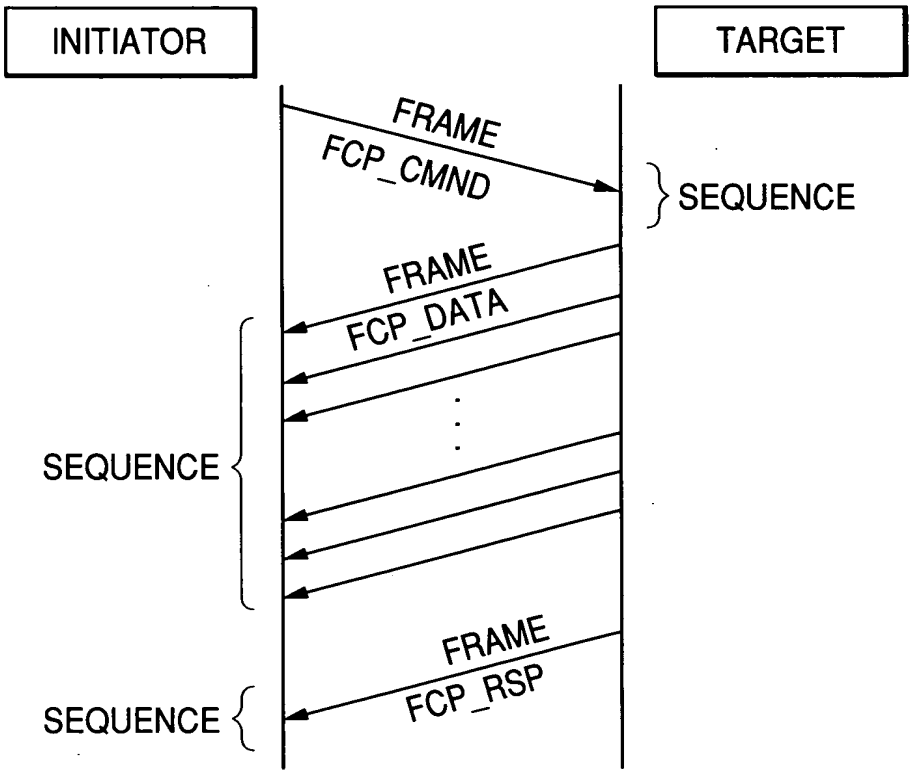
INITIATOR
TARGET
FRAME
FCP_CMND
SEQUENCE
FRAME
FCP_DATA
SEQUENCE
FRAME
FCP_RSP
SEQUENCE

FIG. 24

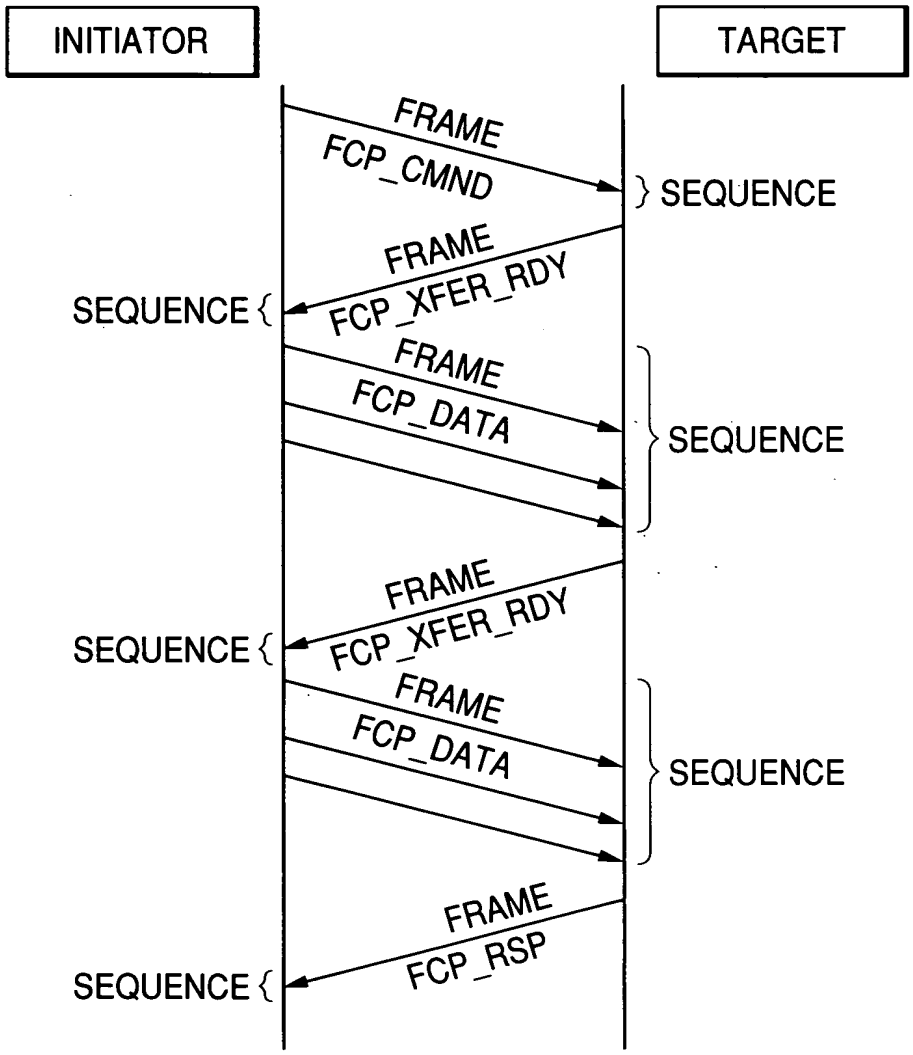
INITIATOR
TARGET
FRAME
FCP_CMND
SEQUENCE
FRAME
FCP_XFER_RDY
SEQUENCE
FRAME
FCP_DATA
SEQUENCE
FRAME
FCP_XFER_RDY
SEQUENCE
FRAME
FCP_DATA
SEQUENCE
FRAME
FCP_RSP
SEQUENCE

FIG. 25

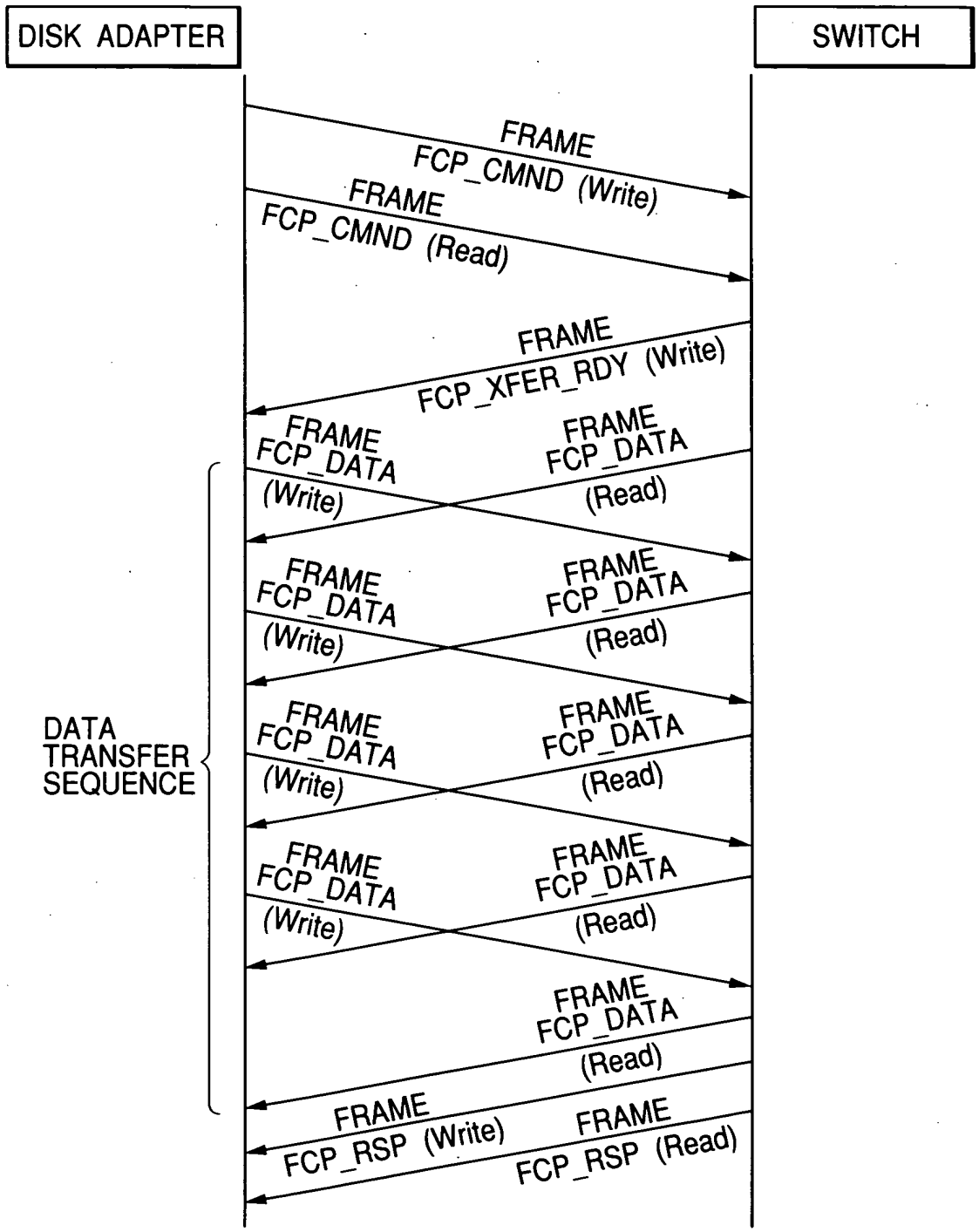
DISK ADAPTER
SWITCH
FRAME FCP_CMND (Write)
FRAME FCP_CMND (Read)
FRAME FCP_XFER_RDY (Write)
FRAME FCP_DATA (Write)
FRAME FCP_DATA (Read)
FRAME FCP_DATA (Write)
FRAME FCP_DATA (Read)
FRAME FCP_DATA (Write)
FRAME FCP_DATA (Read)
FRAME FCP_DATA (Write)
FRAME FCP_DATA (Read)
FRAME FCP_DATA (Read)
DATA TRANSFER SEQUENCE
FRAME FCP_RSP (Write)
FRAME FCP_RSP (Read)

FIG. 26

			WITHOUT FAILURE			WHEN SW1 FAILS		WHEN SW2 FAILS	
DRIVE NO.	VDEV	DKA NO.	DKA Port	Read Drive Port	Write Drive Port	DKA Port	R/W Drive Port	DKA Port	R/W Drive Port
0	0	0	0	PID_0. a	PID_0. b	1	PID_0. b	0	PID_0. a
1				PID_1. b	PID_1. a		PID_1. b		PID_1. a
2				PID_2. a	PID_2. b		PID_2. b		PID_2. a
3				PID_3. b	PID_3. a		PID_3. b		PID_3. a
4	1	1	0	PID_4. a	PID_4. b	0	PID_4. b	1	PID_4. a
5				PID_5. b	PID_5. a		PID_5. b		PID_5. a
6				PID_6. a	PID_6. b		PID_6. b		PID_6. a
7				PID_7. b	PID_7. a		PID_7. b		PID_7. a
8	2	0	1	PID_8. a	PID_8. b	1	PID_8. b	0	PID_8. a
9				PID_9. b	PID_9. a		PID_9. b		PID_9. a
10				PID_10. a	PID_10. b		PID_10. b		PID_10. a
11				PID_11. b	PID_11. a		PID_11. b		PID_11. a
12	3	1	1	PID_12. a	PID_12. b	0	PID_12. b	1	PID_12. a
13				PID_13. b	PID_13. a		PID_13. b		PID_13. a
14				PID_14. a	PID_14. b		PID_14. b		PID_14. a
15				PID_15. b	PID_15. a		PID_15. b		PID_15. a
16	4	0	0	PID_16. a	PID_16. b	1	PID_16. b	0	PID_16. a
17				PID_17. b	PID_17. a		PID_17. b		PID_17. a
18				PID_18. a	PID_18. b		PID_18. b		PID_18. a
19				PID_19. b	PID_19. a		PID_19. b		PID_19. a
20	5	1	0	PID_20. a	PID_20. b	0	PID_20. b	1	PID_20. a
21				PID_21. b	PID_21. a		PID_21. b		PID_21. a
22				PID_22. a	PID_22. b		PID_22. b		PID_22. a
23				PID_23. b	PID_23. a		PID_23. b		PID_23. a
24	6	0	1	PID_24. a	PID_24. b	1	PID_24. b	0	PID_24. a
25				PID_25. b	PID_25. a		PID_25. b		PID_25. a
26				PID_26. a	PID_26. b		PID_26. b		PID_26. a
27				PID_27. b	PID_27. a		PID_27. b		PID_27. a
28	7	1	1	PID_28. a	PID_28. b	0	PID_28. b	1	PID_28. a
29				PID_29. b	PID_29. a		PID_29. b		PID_29. a
30				PID_30. a	PID_30. b		PID_30. b		PID_30. a
31				PID_31. b	PID_31. a		PID_31. b		PID_31. a